Available online at www.sciencedirect.com

SciVerse ScienceDirect

Procedia Engineering 30 (2012) 210 – 217

Procedia Engineering

www.elsevier.com/locate/procedia

International Conference on Communication Technology and System Design 2011

Noise and Error Analysis and Optimization of a CMOS Latched Comparator

Santosh Kumar Patnaik[a], Swapna Banerjee[b], a*

[ab]*Electronics and Electrical Communication Engineering Department, Indian Institute of Technology, Kharagpur-721302, India*

Abstract

In a high speed latched comparator the minimum amount of differential voltage at the input can be detected correctly at the output of the comparator if it does not get affected by the noises and errors generated inside the comparator. To improve the performance of the latched comparator, all the noises and errors should be minimized. In this paper, an attempt has been made to reduce the noises and errors generated within the latched comparator by introducing extra circuit elements. The noise and error optimized comparator shows an improvement in the effective resolution from 7.46-bit to 8.3-bit.

Keywords: Offset error,;Kickback noise,;Metastability; Deterministic offset; Random offset.

1. Introduction

Because of the high speed operation, low power consumption and rail-to-rail output swing, latched comparators are very much suitable for high speed Analog-to-Digital Converters (ADC) [1]. The high speed and rail-to-rail output swing are obtained due to the positive feedback mechanism present in the latched comparators. In addition to the high speed operation and low power consumption, good resolution of the latched comparator is very much essential in order to improve the performance of the latched comparator. This parameter of the comparator gets affected due to the noise and errors generated within the comparator [1]. The noise and errors which affect the performance of the comparator so far the circuit is concerned are: kickback noise, offset error, and metastability error. In a latched comparator, kickback noise arises due to the feed-through of the large voltage transitions through the parasitic coupling capacitors at a particular node to the input port disturbing the input signal [2]. Offset error occurs due to the lack of symmetry of the latched comparator circuitry [3]. This offset error limits the minimum

Santhosh Kumar Patnaik: Tel :9434151273;
E-mail address: skpatnaik@ece.iitkgp.ernet.in

1877-7058 © 2011 Published by Elsevier Ltd. Open access under CC BY-NC-ND license.
doi:10.1016/j.proeng.2012.01.853

achievable comparator resolution. In other words, the input signal whose amplitude is smaller than the input offset voltage will not be correctly detected by the comparator. The offset error has two different components; deterministic offset and random offset. Deterministic offset is due to asymmetries in the comparator circuit itself. Consequently, the output voltage at the quiescent point will be typically different from zero. On the other hand, random offset contemplates asymmetries caused by random deviations of the transistor sizes and technological parameters, and it is observed in both asymmetrical and symmetrical circuit topologies [1]. Metastability error in a latched comparator occurs when a range of input voltages for which the comparator prevents the generation of valid logic outputs in the allotted time slot for regeneration [4]. In order to improve the performance of the latched comparator, all these noise and errors mentioned above needs to be minimized. In this paper, an attempt has been made to analyze the noise and error sources of the latched comparator and by optimizing that, performance of the comparator has been improved.

The subsequent sections have been arranged in the following manner. Section 2 describes the different architectures of the latched comparator. Error and noise optimizations are discussed in Section 3. Section 4 elaborates the full circuit implementation and results. Finally, Section 5 concludes the paper.

2. Architectures of latched comparator

Many latched comparator circuits have already been presented in the literatures to obtain high speed, good resolution with low power consumption. Depending upon these parameters, four different architectures of latched comparator are illustrated in figure 1.

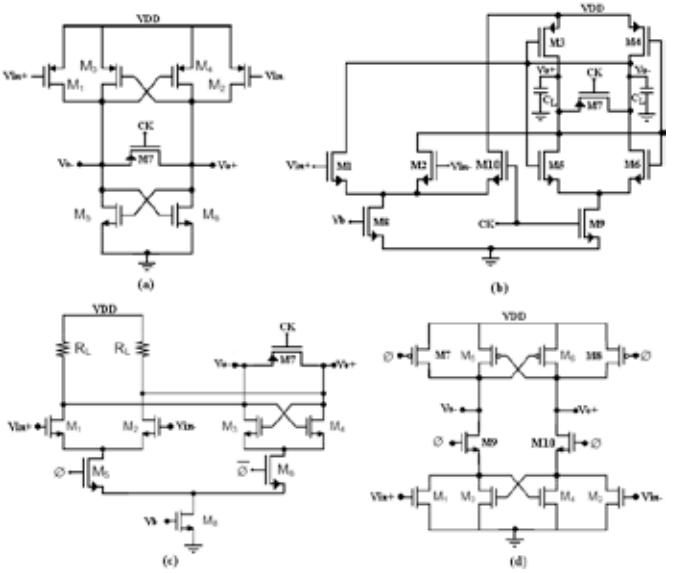

Fig. 1. Architectures of latched comparator

The latched comparator shown in figure 1(a) produces full CMOS logic level due to active pull-up and pull-down. This comparator operates at a very high speed but the power consumption is also large [5]. The latched comparator shown in figure 1(b) produces rail-to-rail logic level and consumes low power. In this comparator, the pull-up is not as fast as in the comparator shown in

figure 1(a), hence, it operates at lower speed compared to the comparator shown in figure 1(a) [1]. The latched comparator shown in figure 1(c) does not produce full logic level, therefore, needs an extra circuit at the output for obtaining the full logic level [6]. The latched comparator shown in figure 1(d) consumes low power and generates full swing at the output but the speed of operation is very slow [7].

Due to the low power consumption, rail-to-rail output swing and comparatively high speed of operation, the latched comparator shown in figure 1(b) has been selected for doing the noise and error analysis. This latched comparator consists of a differential pair M_1-M_2 and a latch pair M_5-M_6, both sharing the cross coupled load M_3-M_4. There are two operating phases of this latched comparator: tracking phase and latching phase. During the tracking phase, the clock signal "CK" is low making transistor M_9 "off" which prevents any current flow through M_5-M_6. Also, in this phase the equalization transistor switch M_7 turns "on" which along with M_3-M_4 forms the load to the differential pair M_1-M_2. In the latching phase, the clock signal "CK" becomes high turning "off" M_7 and turning "on" M_9. This makes M_3-M_5 and M_4-M_6 as two back-to-back CMOS inverters that regenerate the small output voltage to full-scale digital levels. The simplified small signal model of the latched comparator shown in figure 1(b) is illustrated in figure 2 [3]. The corresponding output voltage can be derived as given below.

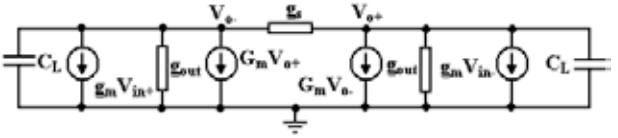

Fig. 2. Simplified small signal model of latched comparator

$$V_{out} = \frac{g_m}{2g_S + g_{out} - G_m} V_{in} + \left(V_{out,0} - \frac{g_m}{2g_S + g_{out} - G_m} V_{in} \right) e^{t/\tau} \qquad (1)$$

where $V_{in} = V_{in+} - V_{in-}$ $V_{out} = V_{o+} - V_{o-}$, $V_{in} = V_{in+} - V_{in-}$, and $\tau = \frac{C_L}{G_m - 2g_S - g_{out}}$.

In equation (1), $V_{out,0}$ is the initial voltage of the output voltage V_{out}, g_m is the transconductance of M_1-M_2, g_{out} is the output admittance of M_1-M_2, g_S is the admittance of the switching transistor M_7, and G_m is the transconductance of the inverter (M_3-M_5 and M_4-M_6) present in the regeneration latch. As is evident from equation (1), only one pole is there at the output node which increases the speed of regeneration.

3. Error and noise analysis and optimization

In this section we have analyzed the effect of the kickback noise, offset error and the metastability error on the performance of the latched comparator shown in figure 1(b). Also, different methods have been adapted to optimize the noise and errors to improve the performance of the latched comparator.

3.1 Offset error

To minimize the offset error due to mismatches in the components present in the latched comparator shown on figure 1(b), an offset cancellation negative feedback-loop circuit has been added. The modified latched comparator circuit is shown in figure 3(a).

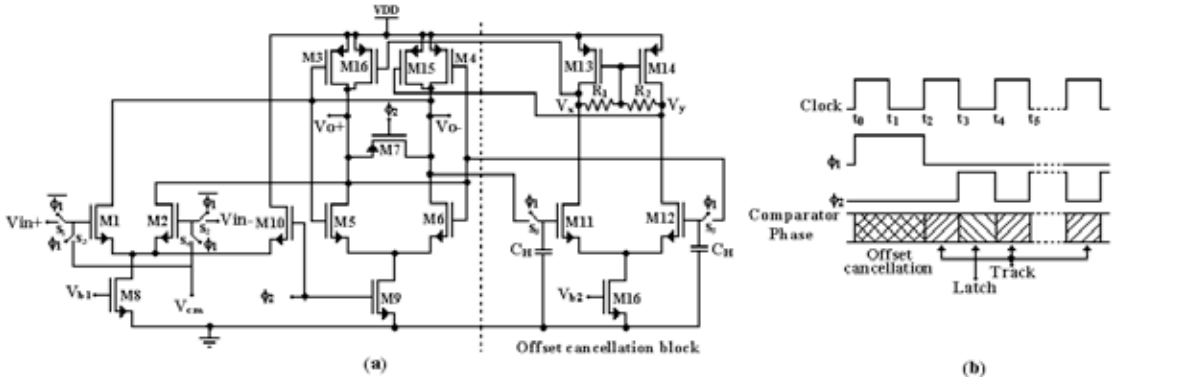

Fig. 3. (a) Latched comparator with offset cancellation circuit; (b) Timing diagram

This comparator works in three different phases: offset cancellation phase, tracking phase and latching phase. In the offset cancellation phase, ϕ_1 becomes high and ϕ_2 becomes low which causes switches S_3 and S_4 to be closed. So, the input signal of the latched comparator is subjected to V_{cm}, the common mode voltage. At the same time the switches S_5 and S_6 are getting closed bringing the offset cancellation block into action. The offset cancellation feedback-loop consists of a differential pair with active load. Its common mode voltage is set by resistive common mode feedback R_1 and R_2. When ϕ_1 moves to logic low with ϕ_2 at logic low state, offset cancellation phase stops and tracking phase starts. With the change in the level of ϕ_2 from logic low to logic high state, regeneration phase starts. The complete operation of the comparator through the timing diagram is shown in figure 3(b). At the end of the offset cancellation phase, the equivalent input referred offset voltage for the circuit shown in figure 3(a) is given as [3];

$$V_{off,in} = \frac{V_{off,out}}{A_v} = \frac{2g_S + g_{out} - G_m}{2g_S + g_{out} + G_{mf} - G_m} V_{off} \qquad (2)$$

To reduce the input referred offset voltage, the numerator of equation (2) has been increased by choosing appropriate regeneration switch size in comparison with back-to-back inverter size to minimize ($2g_S + g_{out} - G_m$) term [3]. Figure 4(a) shows the Monte-Carlo simulation results of the input referred offset error without offset cancellation using negative feedback-loop for 100 samples. The simulation result shows that the maximum value of the offset error without compensation is 73.24mV and the minimum value is -63.23mV. The standard deviation is 30.631mV.

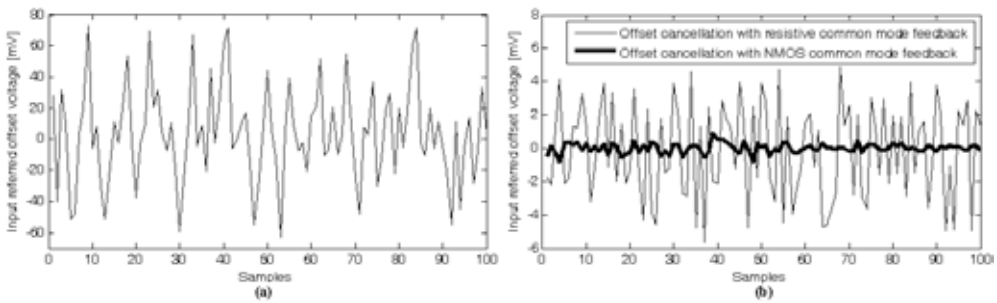

Fig. 4. Simulation results of the offset error (a) without compensation; (b) with compensation

After the addition of the offset cancellation negative feedback-loop circuit, the maximum value of the offset error has been reduced to 4.92mV and the minimum value has been reduced to -4.96mV as shown in figure 4(b). The standard deviation for this case is 2.851mV. This value of the offset error obtained after the compensation is still large. To reduce it further we have replaced the resistors R_1 and R_2 shown in figure 3(a) with two NMOS transistors. The gates of these NMOS transistors are connected to the supply voltage whereas the common drain is connected to the common gate of active load transistors (M_{13}-M_{14}). This arrangement has further reduced the maximum value of the offset error to 0.876mV and the minimum value of the offset error to -0.792mV. The standard deviation of the offset error is 0.29mV as shown in figure 4(b).

3.2 Kickback noise

Figure 5(a) shows, how the kickback noise is coupled to the input signal through $C_{GD1,2}$ and $C_{GS1,2}$ of the latched comparator. To reduce the kickback noise due to the transient at the regeneration nodes Y_1 and Y_2, the drains of the transistors forming the input differential pair need to be isolated from the regeneration nodes during the regeneration phase [1]. This is done using switching transistors between the regeneration node and the drains of the input differential pair. These switches isolate the regeneration node and the drains of the input differential pair when regeneration starts.

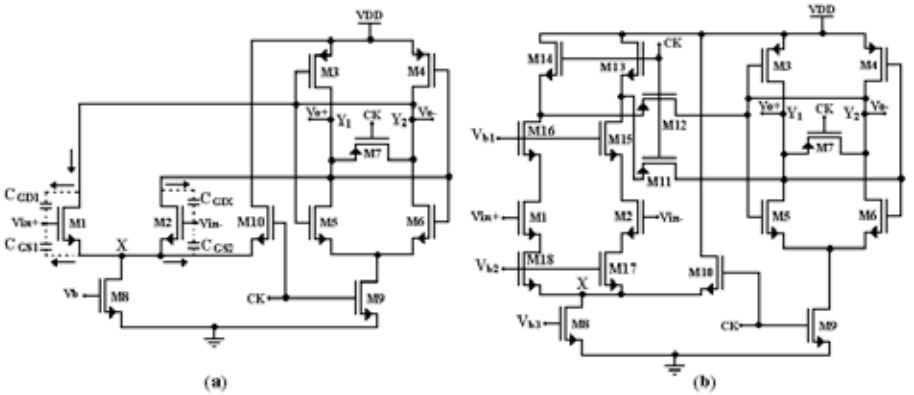

Fig. 5. (a) Kickback noise due to the parasitic capacitance; (b) Kickback noise compensation

The modified latched comparator circuit is shown in figure 5(b). Transistors M_{11} and M_{12} are used as the switches between the regeneration node and the drains of the input differential pair M_1-M_2. In the regeneration phase, M_{11} and M_{12} are "off" blocking the current flow in the input differential pair. However, there is still heavy kickback noise coupled to input nodes as the switching transistors M_{11}-M_{12} are "on" during tracking period. To solve this problem, two more transistors M_{13}-M_{14} are connected as load in the coscode configuration with the input differential pair. These load transistors offer current towards the input differential pair while the switching transistors M_{11}-M_{12} are "off" [2]. To reduce the kickback noise further in the tracking phase, two more transistors M_{15}-M_{16} are connected in cascode configuration above the transistors M_1-M_2. The shielding property of the cascode structure helps in reducing the voltage variation at the drains of the input differential pair. To reduce the kickback noise due to the transients at the common source node X, two more transistors M_{17}-M_{18} are used as the source degeneration transistors. These two transistors help in shielding the transients at the node X from the input signal.

Figure 6 shows the simulation result of the kickback noise. Without any kickback noise compensation, the maximum value of the kickback noise coupled to the input signal is 53.61mV as shown in figure 6(a).

After the addition of the compensation circuit for the kickback noise due to the transients at the regeneration node, the maximum value of the kickback noise has reduced to 17.61mV as shown in figure 6(b). With the compensation circuit for the kickback noise both due to the transients at the regeneration node Y_1-Y_2 and common source node X, the maximum value of the kickback noise has been further reduced to 2.71mV as shown in figure 6(c).

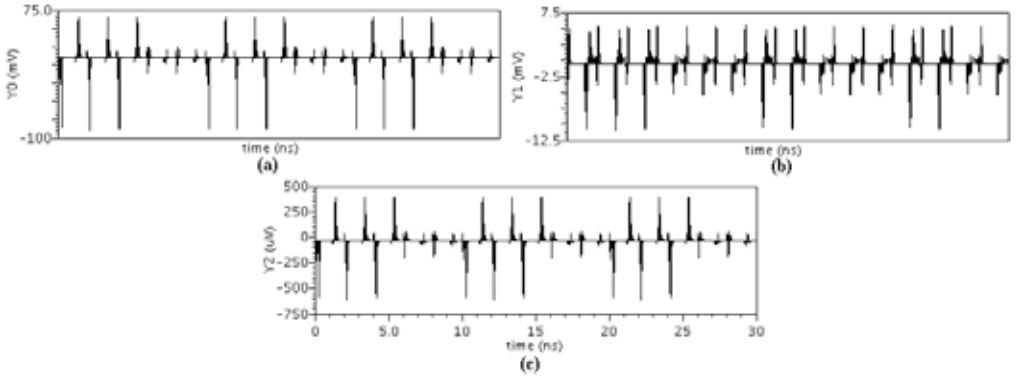

Fig. 6. Simulation results of the kickback noise in the latched comparator

3.3 Metastability error

In the regeneration phase of the latched comparator shown in figure 1(b), G_m is greater than $(2g_S + g_{out})$ [3]. So, the first term in equation (1) can be neglected. Therefore, the output voltage in the regeneration phase is expressed as;

$$V_{out} = V_{out,0} e^{t/\tau} \tag{3}$$

Let v be the smallest starting regeneration value that will not cause an error by time T, and V is the final output voltage of the latched comparator by time T then;

$$v = Ve^{-T/\tau} \tag{4}$$

Let V_R is the maximum amount of change in the voltage at the input of the comparator that can be made without causing a transition in the output of the comparator, the probability of metastability error can be expressed as;

$$P_{error} = \frac{2v}{V_R} \tag{5}$$

Substituting the value of v in equation (5), the probability of metastability error becomes;

$$P_{error} = \frac{2V}{V_R} e^{-T/\tau} \tag{6}$$

The best way to reduce the probability of metastability error is to increase V_R at the input of the latched comparator. This can be achieved by connecting a pre-amplifier having a gain of A_v at the input of the comparator. With this arrangement the probability of metastability error becomes;

$$P_{error} = \frac{2V_L}{A_v V_R} e^{-T/\tau} \tag{7}$$

Therefore, it is evident from equation (7) that the probability of metastability error can be reduced by a factor of A_v in comparison to equation (6) by adding a pre-amplifier before the latch in the latched comparator circuit.

4. Circuit implementation and results

The circuit schematic of the latched comparator with offset error and kickback noise cancellation circuit is shown in figure 7. The front end of this latched comparator is a pre-amplifier which helps in reducing the metastability error and reduces the kickback noise considerably [1]. The next stage is the latch with offset error and kickback noise cancellation circuit, which furnishes supplementary gain to the comparator to generate the logic output. In addition, it provides a stable output synchronous with the clock that brings into operation the regenerative loop. The last stage of the comparator is an output buffer. This plays a very important role in filtering the noise coming from the latch. Due to the hysteresis present in the output buffer, the output transition will take place only when the latch output is sufficiently high or low resulting in sharp, well-defined digital data.

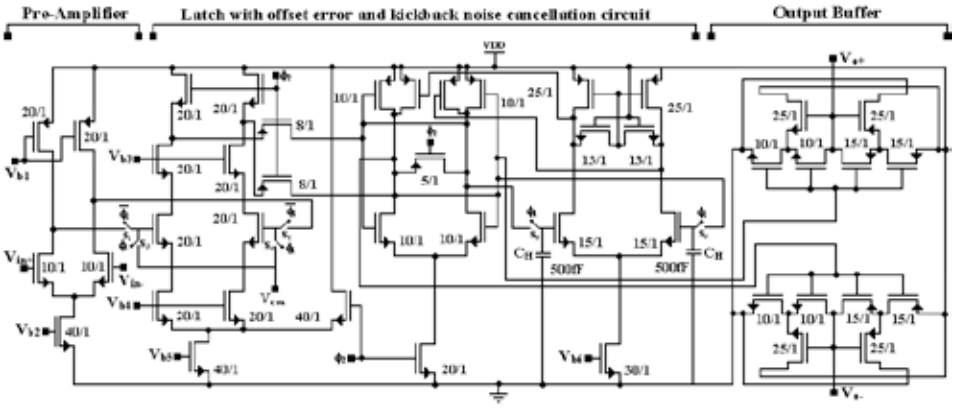

Fig. 7. Circuit schematic of the comparator with offset error and kickback noise cancellation circuitry

Figure 8(a) shows the layout of the latched comparator. Single poly, six metal, 0.18μm CMOS process is used for this purpose. Common centroid layout technique has been adapted at intra- and inter-block levels for obtaining a better matching between the devices [8]. Figure 8(b) shows the post layout simulation result of the noise and error optimized latched comparator. This shows that, the use of hysteresis output buffer results in sharp well defined digital data by filtering switching noises coming from the latched comparator. The comparison of the performance parameters of this comparator with the comparators mentioned in [2] and [3] are summarized in Table 1.

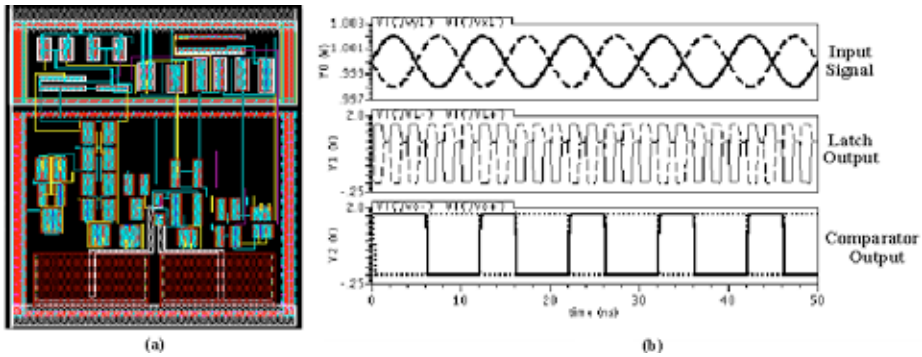

Fig. 8. (a) Layout; (b) Simulation result

Table 1. Comparison of the performance parameters of the comparators

References	Technology	Speed of operation	Offset error	Kickback noise	Resolution	Power dissipation
[2]	0.18µm CMOS	250MHz	4mV	0.5mV	8-bit	193µW
[3]	0.18µm CMOS	500MHz	200µV	-	-	600µW
This work	0.18µm CMOS	500MHz	0.29mV	2.71mV	8-bit	337µW

5. Conclusions

In this paper, we have analyzed the effect of kickback noise, offset error and the metastability error on the performance of a high speed latched comparator. The offset error of the comparator has been reduced by adding an offset cancellation negative feedback loop circuit. This addition of the offset cancellation negative feedback loop circuit reduced the offset error from 30.63mV to 0.29mV. The kickback noise is reduced from 53.61mV to 2.71mV by connecting switching and cascade transistors in the latched comparator. With this, it can be concluded that, the noise and error levels of a latched comparator can be reduced with proper circuit optimization which will improve the performance of the comparator but at the cost of power.

References

[1] B. Razavi, “Principles of Data Conversion System Design”, AT&T Bell laboratories, IEEE Press, 1995.
[2] Y. Qi, G. Zhang, Z. Shao, and B. Wang, “A low kick back noise latched comparator for high speed folding and interpolating ADC”, APCCAS, Nov. 2008. p. 272-275.
[3] K. D. Sadeghipour, “An improved low offset latch comparator for high-speed ADCs”, Analog Integr Circ Sig Process, vol. 66, no. 2, 2011, p. 205-212.
[4] C. L. Portmann, “Characterization and Reduction of Metastability Errors in CMOS Interface Circuits”, Technical Report, June 1995.
[5] B. Razavi, and B. A.Wooley,“Design techniques for high-speed, high resolution comparators”, IEEE J. Solid-State Circuits, vol. 27, no. 12, December 1992, p. 1916-1926.
[6] F. Maloberti, “Analog Design For Cmos Vlsi Systems”, Kluwer Academic Publishers, 2001.
[7] A. Yukawa, “A CMOS 8-Bit High-Speed A/D Converter IC”, IEEE JSSC, vol. 20, issue 3, 1985. p. 775-779.
[8] Alan Hastings, “The Art of Analog Layout”, Prentice Hall, 2001.